AMENDMENT TO CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-36 (cancelled)

Claim 37 (Currently Amended) A method, comprising:

partitioning a program into a plurality of groups of instructions;

assigning a group of instructions selected from the plurality of groups of instructions partitioned from the program to a plurality of interconnected preselected computation nodes;

loading a subset of instructions of the assigned group of instructions into a frame of buffers spanning the plurality of interconnected preselected computation nodes having been assigned the group of instructions; and

executing the subset~~group~~ of instructions as each one of the instructions in the ~~group~~ subset of instructions loaded into the frame of spanning buffers receives all necessary associated operands for execution.

Claim 38 (Previously presented) The method of claim 37, wherein at least one computation node included in the plurality of interconnected preselected computation nodes has at least one input port capable of being coupled to at least one preselected first other computation node included in the plurality of interconnected preselected computation nodes, the input port to receive input data, a first store coupled to the at least one input port to store the input data, a second store coupled to an instruction sequencer, the second store to receive and store the at least one instruction, an instruction wakeup unit to match the input data to the at least one instruction, at least one execution unit to execute the at least one instruction using the input data to produce output data, at least one output port capable of being coupled to at least one second other preselected computation node included in the plurality of interconnected preselected computation nodes, and a router to direct the output data from the at least one output port to the at least one preselected second other computation node.

Claim 39 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is a basic block.

Claim 40 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is a hyperblock.

Claim 41 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is a superblock.

Claim 42 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is an instruction trace constructed by a hardware trace construction unit at run time.

Claim 43 (Currently amended) The method of claim 37, wherein loading the subset~~group~~ of instructions into a frame of buffers spanning the plurality of interconnected preselected computation nodes includes:
sending at least two instructions selected from the group of instructions from an instruction sequencer to a selected computation node included in the plurality of interconnected preselected computation nodes for storage in a store.

Claim 44 (Currently Amended) The method of claim 37, wherein executing the ~~group~~ subset of instructions loaded into the frame of spanning buffers as each one of the instructions in the ~~group~~ subset of instructions receives all necessary associated operands for execution includes:
matching at least one instruction selected from the subset~~group~~ of instructions with at least one operand received from an other computation node included in the plurality of interconnected preselected computation nodes.

Claim 45 (Cancelled)

Claim 46 (Currently amended) The method of claim 37, further comprising~~wherein~~ concurrently assigning another group of instructions selected from the plurality of groups of instructions to

another or the same plurality of interconnected preselected computation nodes ~~includes:~~ for concurrent execution using one or more other frames of buffers spanning the another or fame plurality of interconnected preselected computation nodes.

~~assigning a first group of instructions to a first set of frames included in the plurality of interconnected preselected computation nodes;~~

~~assigning a second group of instructions to a second set of frames included in the plurality of interconnected preselected computation nodes,~~ wherein the ~~first group and the second~~two groups of instructions are capable of concurrent execution~~, and wherein at least one output datum associated with the first group of instructions is written to a register file and passed directly to the second group of instructions for use as an input datum by the second group of instructions~~.

Claim 47 (Currently amended) An article comprising a machine-accessible medium having machine executable instructions stored~~associated data~~ therein, ~~wherein the data, when accessed, results in a machine performing~~ configured to enable a machine to:

load~~ing~~ a subset of a group of instructions selected from a plurality of groups of instrcutions partitioned from a program, to a frame of buffers spanning a plurality of interconnected preselelcted computation nodes, ~~wherein a program is partitioned into a plurality of groups~~to execute the subset of instructions, wherein the group of instructions ~~from the plurality of groups of instructions~~ is assigned to be executed by the plurality of interconnected preselelcted computation nodes~~; and~~

~~executing the group of instructions as each one of the instructions in the group of instructions receives all necessary associated operands for execution~~.

Claim 48 (Previously presented) The article of claim 47, wherein partitioning the program into the plurality of groups of instructions is performed by a compiler.

Claim 49 (Previously presented) The article of claim 47, wherein partitioning the program into the plurality of groups of instructions is performed by a run-time trace mapper.

Claim 50 (Currently amended) The article of claim 47, wherein the machine-accessible medium further includes ~~data, which when accessed by the machine, results in~~ instructions configured to enable the machine ~~performing:~~
to statically assign~~ing all~~ each of the plurality of groups of instructions to a plurality of interconnected preselected computation nodes for execution.

Claim 51 (Cancelled)

Claim 52 (Currently amended) The article of claim 47, wherein the machine-accessible medium further includes ~~data, which when accessed by the machine, results in~~instructions configured to enable the machine ~~performing:~~to
generate~~ing~~ a wakeup token to reserve an output data channel to connect selected computation nodes included in the plurality of interconnected preselected computation nodes.

Claim 53 (Currently amended) The article of claim 47, wherein the machine-accessible medium further includes ~~data, which when accessed by the machine, results in~~instructions configured to enable the machine ~~performing:~~ to repeat said loading until the entire group of instructions are executed, and to detect~~ing~~ execution termination of the group of instructions including an output having architecturally visible data; and committing the architecturally visible data to a register file.

Claim 54 (Currently amended) The article of claim 47, wherein the machine-accessible medium further includes instructions configured to enable the machine to repeat said loading until the entire group of instructions are executed, and to~~data, which when accessed by the machine, results in the machine performing:~~ detect~~ing~~ execution termination of the group of instructions including an output having architecturally visible data; and committing the architecturally visible data to a memory.

Claim 55 (Currently amended) The article of claim 47, wherein the machine-accessible medium further instructions configured to enable ~~includes data, which when accessed by the machine, results in~~ the machine ~~performing:~~to

routeing an output datum arising from executing one of the ~~group~~ subset of instructions to a consumer node included in the plurality of interconnected preselected computation nodes, wherein the address of the consumer node is included in a token associated with at least one instruction included in the ~~group~~ subset of instructions.

Claim 56 (New) The method of claim 37 futher comprising repeating said loading and exeucting until the entire group of instructions have been executed.

Claim 57 (New) An apparatus, comprising:

a processor; and

storage medium coupled to the processor and having first instructions stored therein to be executed by the processor, wherein the first instructions are configured to

partition a program into a plurality of groups of second instructions;

assign a group of second instructions selected from the plurality of groups of second instructions partitioned from the program to a plurality of interconnected preselected computation nodes; and

causing a subset of the second instructions of the assigned group of second instructions to be loaded into a frame of buffers spanning the plurality of interconnected preselected computation nodes having been assigned the group of second instructions, wherein the subset of second instructions are executed as each one of the instructions in the subset of second instructions loaded into the frame of spanning buffers receives all necessary associated operands for execution.

Claim 58 (New) The apparatus of claim 57, wherein at least one of the plurality of groups of second instructions is a selected of one a basic block, a hyperblock or a superblock.

Claim 59 (New) An apparatus, comprising:

computing resource including an execution unit configured to execute instructions; and

interconnect resource coupled to the computing resource to enable the apparatus to be a member of a group of interconnected computation nodes preselected to execute a group of instructions by successively executing subgroups of the group of instructions;

wherein the interconnect resource includes:

at least one input port capable of being coupled to at least a first other preselected computation node included in the plurality of interconnected preselected computation nodes, the input port to receive input data,

a first store coupled to the at least one input port to store the input data,

a second store coupled to the execution unit, the second store to receive and store at least one instruction of a subgroup, the second store being a part of a frame of buffers spanning the plurality of interconnected preselected computation nodes to store a subgroup of instructions,

an instruction wakeup unit to match the input data to the at least one stored instruction,

at least one output port coupled to the execution unit and capable of being coupled to at least one second other preselected computation node included in the plurality of interconnected preselected computation nodes, and

a router to direct an output data of the execution unit from the at least one output port to the at least one preselected second other computation node.

Claim 60 (New) A system, comprising:

a plurality of interconnected computing nodes configured to be pre-selectable to cooperatively execute a group of instructions;

wherein each of the interconnect computing nodes includes:

computing resource including an execution unit configured to execute instructions; and

interconnect resource coupled to the computing resource to enable the computing node to cooperate with the other interconnected computation nodes to execute the group of instructions by successively executing subgroups of the group of instructions;

wherein the interconnect resource includes:

at least one input port capable of being coupled to at least a first other preselected computation node included in the plurality of

interconnected preselected computation nodes, the input port to receive input data,

a first store coupled to the at least one input port to store the input data,

a second store coupled to the execution unit, the second store to receive and store at least one instruction of a subgroup, the second store being a part of a frame of buffers spanning the plurality of interconnected preselected computation nodes to store a subgroup of instructions,

an instruction wakeup unit to match the input data to the at least one stored instruction,

at least one output port coupled to the execution unit and capable of being coupled to at least one second other preselected computation node included in the plurality of interconnected preselected computation nodes, and

a router to direct an output data of the execution unit from the at least one output port to the at least one preselected second other computation node.